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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,557	03/12/2004	Santanu Chaudhuri	INTEL-0071	6472
34610 7590 10/17/2007 KED & ASSOCIATES, LLP P.O. Box 221200 Chantilly, VA 20153-1200			EXAMINER FLORES, LEON	
			ART UNIT 2611	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/798,557

Applicant(s)

CHAUDHURI ET AL.

Examiner

Leon Flores

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 02 August 2007.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-34 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-34 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)

Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)

Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. **Claims (1-4, 6, 8-16, 18, 20-25, 27-30 & 34) rejected under 35 U.S.C. 103(a) as being unpatentable over Dally (US Publication 2001/0026595 A1) in view of John G. Proakis (hereinafter Proakis), "Digital Communications", fourth edition, 2000.**

Re claim 1, Dally discloses a circuit, comprising: a detector to detect loss in a link coupled to a transmitter (See fig. 1: 24 & paragraphs 51-53); and a controller to automatically determine a multi-tap equalization setting based on the loss detected in the link coupled to the transmitter (See fig. 1: 26 & paragraphs 51-53).

But the reference of Dally fails to explicitly teach an equalizer to generate a pulse signal to equalize transmission of data on the link based on the multi-tap equalization setting, the pulse signal having a plurality of levels that respectively correspond to at least one pre-cursor and at least one post-cursor of a main pulse, the transmission of said data to be equalized based on the at least one pre-cursor and at least one post-cursor.

However, Proakis does. (See section 11.2 & figure 11.2-1) Proakis discloses a decision feedback equalizer capable of reducing pre-cursor and post-cursor interferences.

Therefore, taking the combined teachings of Dally and Proakis as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated a decision feedback equalizer into the system of Dally, in the manner as claimed and as taught by Proakis, for the benefit of reducing pre-cursor and post-cursor interferences.

Re claim 2, the combination of Dally and Proakis discloses that wherein the equalization setting is a two-tap equalization setting. (In Dally, see paragraph 45)

Re claim 3, the combination of Dally and Proakis discloses that wherein the equalization setting is a five-tap equalization setting. (In Dally, see paragraph 36)

Re claim 4, the combination of Dally and Proakis discloses that wherein the detector is to detect loss in the link based on a signal which includes link loss

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information received through a predetermined channel. (In Dally, see fig. 1: 24 & paragraphs 51-53)

Re claim 6, the combination of Dally and Proakis discloses that wherein the controller determines the equalization setting during link initialization. (In Dally, see paragraph 51)

Claim 8 is a method claim corresponding to system claim 1. Hence, the steps performed in method claim 8 would have necessitated the elements in system claim 1. Therefore, claim 8 has been analyzed and rejected w/r to claim 1 above.

Claim 9 is a method claim corresponding to system claim 2. Hence, the steps performed in method claim 9 would have necessitated the elements in system claim 2. Therefore, claim 9 has been analyzed and rejected w/r to claim 2 above.

Claim 10 is a method claim corresponding to system claim 3. Hence, the steps performed in method claim 10 would have necessitated the elements in system claim 3. Therefore, claim 10 has been analyzed and rejected w/r to claim 3 above.

Re claim 11, the combination of Dally and Proakis discloses that wherein measuring the loss is performed at the receiver. (In Dally, see paragraphs 52-53)

Re claim 12, the combination of Dally and Proakis discloses that wherein measuring the loss includes: transmitting a clock signal from the transmitter to the receiver; and computing the loss as a ratio of the transmitted clock signal amplitude and the received clock signal amplitude. (In Dally, see paragraphs 51-53)

Re claim 13, the combination of Dally and Proakis discloses that wherein the receiver receives the clock signal through an input which is offset calibrated. (In Dally, see paragraph 52)

Re claim 14, the combination of Dally and Proakis discloses that wherein the receiver sweeps the offset to determine the amplitude of the received clock signal to within a predetermined error. (In Dally, see paragraph 52)

Re claim 15, the combination of Dally and Proakis discloses that wherein the predetermined error is one LSB error. (In Dally, see paragraph 52)

Re claim 16, the combination of Dally and Proakis discloses that wherein the loss is measured based on the following equation: $\text{Loss (dB)} = -20 \log \left(\frac{N_{Ac}}{N_{oc}} \right) \cdot \left(\frac{V_{dc_eq}}{V_{swing}} \right)$ where N_{Ac} is a number of steps to determine the amplitude of the received clock signal, N_{oc} is a number of steps to determine a voltage swing of a DC voltage transmitted to the receiver, V_{dc_eq} is an equalized DC voltage, and V_{swing} is the voltage swing. (In Dally, see paragraph 52. Furthermore, one skilled

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in the art would know how to make and use this formula by performing tests between the transmitter and receiver.)

Claim 18 is a method claim corresponding to system claim 6. Hence, the steps performed in method claim 18 would have necessitated the elements in system claim 6. Therefore, claim 18 has been analyzed and rejected w/r to claim 6 above.

Claim 20 has been analyzed and rejected w/r to claim 1 above.

Re claim 21, the combination of Dally and Proakis discloses that wherein the first circuit includes a chipset and the second circuit includes a CPU. (In Dally, see paragraph 26 and claim 50.)

Re claim 22, the combination of Dally and Proakis discloses that wherein the first circuit includes a chipset and the second circuit includes a memory. (In Dally, see fig. 1 & paragraph 43)

Re claim 23, the combination of Dally and Proakis discloses that wherein the memory is one of a RAM and a cache. (In Dally, see paragraph 43)

Re claim 24, the combination of Dally and Proakis discloses that wherein the first circuit includes a memory and the second circuit includes a CPU. (In Dally, see fig. 1 & paragraph 43)

Re claim 25, the combination of Dally and Proakis discloses that wherein the first circuit includes a graphical interface and the second circuit includes at least one of a memory, CPU, and chipset. (These are inherent features in typical digital system.)

Claim 27 has been analyzed and rejected w/r to claim 6 above.

Claim 28 has been analyzed and rejected w/r to claim 1 above.

Claim 29 has been analyzed and rejected w/r to claim 6 above.

Claim 30 has been analyzed and rejected w/r to claim 7 above.

Re claim 34, the combination of Dally and Proakis discloses that wherein said data is to be transmitted between the transmitter and another circuit, the transmitter and other circuit residing on a same circuit board. (In Dally, see fig. 1)

Claims (7 & 19) are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally (US Publication 2001/0026595 A1) and John G. Proakis (hereinafter Proakis), "Digital Communications", fourth edition, 2000, as applied to claim 1 above, and further in view of Schmidt et al. (hereinafter Schmidt) (US Patent 7,130,343 B2)

Re claim 7, the combination of Dally and Proakis fails to disclose that wherein at least one of the equalizer or the controller receives information indicative of voltage and timing margins of an eye diagram at a receiver and adjusts the equalization setting based on the voltage and timing margins. (In Schmidt, see fig. 2 & col. 3, lines 40-45)

However, Schmidt does. (See fig. 2 & col. 3, lines 40-45) Schmidt discloses a decision feedback equalizer DFE capable of reducing both pre-cursor and post-cursor interferences in the received signal. The coefficients of the equalizer are adjusted by the filter controller.

Therefore, taking the combined teachings of Dally and Schmidt as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated a decision feedback equalizer into the system of Dally, in the manner as claimed and as taught by Schmidt, for the benefit of reducing pre-cursor and post-cursor interferences.

Claim 19 is a method claim corresponding to system claim 7. Hence, the steps performed in method claim 19 would have necessitated the elements in system claim 7. Therefore, claim 19 has been analyzed and rejected w/r to claim 7 above.

Claims (5, 17, and 26) are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally (US Publication 2001/0026595 A1) and John G. Proakis (hereinafter Proakis), "Digital Communications", fourth edition, 2000, as applied to claim 1 above, and further in view of Fuhrmann et al. (hereinafter Fuhrmann) (US Patent 5,991,308)

Re claim 5, the combination of Dally and Proakis further discloses a look-up table to store a plurality of predetermined tap coefficient settings that correspond to a respective number of link loss values (In Dally, see paragraph 44).

But they fail to teach the control circuit to search the look-up table for a tap coefficient setting that corresponds to the detected link loss, the levels in the pulse signal respectively corresponding to tap coefficients included in the setting produced by the search.

However, Fuhrmann does. (See col. 93, lines 58-63) Fuhrmann discloses a forward feedforward and a decision feedback equalizer used to compensate for pre-cursor and post-cursor interferences, respectively. The tap weights used to compensate for these impairments are stored in a memory by a LMS. The CPU reads the tap weights and transmits them to a remote unit.

Therefore, taking the combined teachings of Dally, Proakis and Fuhrmann as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Dally, as modified by Proakis, in the manner as claimed and as taught by Fuhrmann, for the benefit of reducing pre-cursor and post-cursor interferences.

Claim 17 is a method claim corresponding to system claim 5. Hence, the steps performed in method claim 17 would have necessitated the elements in system claim 5. Therefore, claim 17 has been analyzed and rejected w/r to claim 5 above.

Claim 26 has been analyzed and rejected w/r to claim 5 above.

Claims (31-32) are rejected under 35 U.S.C. 103(a) as being unpatentable over Dally (US Publication 2001/0026595 A1) and John G. Proakis (hereinafter Proakis), "Digital Communications", fourth edition, 2000, as applied to claim 1 above, and further in view of Kakuishi et al. (hereinafter Kakuishi) (US Patent 5,481,564)

Re claim 31, the combination of Dally and Proakis fails to specifically disclose that wherein one or more levels of the pulse signal that correspond to the at least one pre-cursor have a first polarity and one or more levels of the pulse signal that correspond to the at least one post-cursor have a second polarity opposite to the first polarity.

However, Kakuishi does. (See fig. 6 & col. 5, lines 1-7) Kakuishi discloses an equalizer capable of eliminating intersymbol interference in a received signal. The tap coefficients responsible for reducing these impairments are the same as these interference components.

Therefore, taking the combined teachings of Dally, Proakis and Kakuishi as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Dally, as modified by Proakis, in the manner as claimed and as taught by Kakuishi, for the benefit of reducing pre-cursor and post-cursor interferences.

Re claim 32, the combination of Dally, Proakis and Kakuishi discloses that wherein the one or more levels of the pulse signal that having the second polarity substantially negate a first-polarity component of the main pulse. (In Kakuishi, see fig. 6 & col. 5, lines 1-7)

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dally (US Publication 2001/0026595 A1) and John G. Proakis (hereinafter Proakis), "Digital Communications", fourth edition, 2000, as applied to claim 1 above, and further in view of Aly et al. (hereinafter Aly) (US Patent 4,995,031)

Re claim 33, the combination of Dally and Proakis fails to specifically disclose that wherein one or more levels of the pulse signal that correspond to the at least one pre-cursor reduce rise-time delay in data transmission noise.

However, Aly does. (See col. 1, line 65 – line 1) Aly discloses an equalizer for reducing pre-cursor and post-cursor interferences. Pre-cursor interference shows the received signal, in the time domain, with a slow rise time.

Therefore, taking the combined teachings of Dally, Proakis and Aly as a whole. It would have been obvious to one of ordinary skills in the art to have incorporated this feature into the system of Dally, as modified by Proakis, in the manner as claimed and as taught by Aly, for the benefit of reducing pre-cursor and post-cursor interferences.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Contact


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF
September 12, 2007


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SUPERVISORY PATENT EXAMINER